3.8 An 80/100MS/s 76.3/70.1dB SNDR ΔΣ ADC for Digital TV Receivers

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In digital TV receivers, the use of high-bandwidth and high-resolution ADCs allows part of the channel-filtering and VGA functions to be performed in the digital domain, which is more suitable for process scaling. This paper presents a wideband ΔΣ ADC with a double sampling technique and OTA optimization methodology, resulting in better distortion performance and lower power consumption. The ΔΣ ADC achieves a 76.3/70.1dB peak SNDR over a 3.2/4MHz bandwidth while consuming 23.8/34.4mW from a 1.8V supply, which leads to a 0.7/1.64pJ/conversion FOM.

The proposed ΔΣ ADC is to be used in direct-conversion receivers for integrated services for digital broadcasting-terrestrial (ISDB-T) and DVB-T. The digital TV signal bandwidth at RF is approximately 6MHz for ISDB-T (8MHz for DVB-T), which leads to a 3MHz (4MHz) bandwidth for the ΔΣ ADC. The choice of the OSR is a trade-off between the anti-alias filtering and the power consumption of the ADC. The OSR of 12 is selected, resulting in 80MHz and 100MHz sampling frequencies (f_S) for 3MHz and 4MHz bandwidths, respectively. A 3rd-order Chebychev I filter fulfills the anti-alias filtering requirement. The SNR is constrained mainly by the required adjacent-channel immunity. The target SNR is determined to be 70dB from the following considerations. The required desired-to-undesired signal ratio (D/U) is -35dB while maintaining a 22dB carrier-to-noise ratio (C/N), the 3rd-order filter provides 5dB attenuation of the undesired signal and 18dB margin is taken.

Figure 3.8.1 shows the architecture of the proposed ΔΣ ADC with a 4th-order feedforward loop-filter and a 4b quantizer. The ΔΣ ADC has a direct feedforward path from the input of the ΔΣ ADC to the quantizer input, which results in the suppression of the input signal component in the loop-filter [1]. Therefore, the integrators process only the quantization noise, improving the distortion performance. However, such architecture requires a delay-free quantizer and DWA logic to cancel out the input signal component at the input subtractor before the loop-filter, and is not appropriate for high-speed applications. In a normal two-phase clocking scheme, the time required for the quantizer and DWA logic to operate, reduces the time available for the integration phase of the first integrator. To alleviate this problem, the proposed modulator employs a double sampling technique at the input of the ΔΣ ADC. Double sampling is equivalent to inserting a half-period delay before the input subtractor. Therefore, the allowable time for the quantizer and DWA logic is relaxed by half a clock period. Also, the required settling time of the buffer driving the sampling capacitors of the ΔΣ ADC can be twice larger. The path mismatch in the double sampling block is not a critical problem, because the OSR is relatively large and interferers around $f_S/2$ present at the modulator input are attenuated by more than 60dB through the anti-alias filter. Furthermore, the number of summing nodes at the switched-capacitor (SC) passive adder before the quantizer is reduced by summing some of the feedforward paths at the input of the last integrator [2]. This reduces the gain loss caused in the passive adder and eases the design of the quantizer.

Figure 3.8.2 shows the SC implementation of the ΔΣ ADC. The input and the feedback DAC capacitors are separated to reduce the input linearity degradation and to reduce the design complexity of the voltage reference buffer. To achieve the necessary linearity, the clock signals applied to the continuous-time input sampling switches are bootstrapped by the circuit shown in [3]. The types of OTA topologies suitable for low-voltage and low-power applications are folded-cascode and current-mirror OTAs, whose input common-mode voltages can be biased to near the ground level, and thus NMOS transistors can be used for the input switches. The current-mirror OTA can make the optimal trade-off between its unity-gain frequency and its thermal noise by the current mirror ratio. Therefore, the current-mirror OTA shown in Fig. 3.8.3 is chosen and implemented in the first integrator. Different from [4], the current mirror ratio of M2 and M3 is limited to less than 2, to reduce the thermal noise contribution of the OTA in the first integrator. Because the integrators process only the shaped quantization noise, their maximum output range is a fraction of the ΔΣ ADC reference level, which reduces the slew rate requirement of the OTA (SR > 120V/μs). Therefore, the current through the input transistor M1 is relatively large (560μA) while the current in the output transistor M3 (or M4) is small (320μA). Part of the current from the input transistor M1 flows through M2c transistors to meet both the high bandwidth and moderate slew-rate requirements.

The prototype chip is fabricated in a 0.18μm 1P5M mixed-signal CMOS process. Figure 3.8.4 shows measured SNR and SNDR as a function of the input signal level at 80MHz f_S for ISDB-T. The peak SNR and SNDR are 78.2dB and 76.3dB, respectively. The dynamic range is 78.5dB. Figure 3.8.4 also shows the output spectrum obtained for a 7.5dBm input at 1MHz, which is the maximum level before the modulator oscillates. No 3rd harmonic is observed. The 2nd-order harmonic is 85dB lower than the fundamental tone. This seems to be due to a mismatch in the thresholds of the 4b quantizer. Due to the parasitic capacitors, the 4th integrator OTA bandwidth seems to be smaller than expected, which leads to the slight peak in the NTF around 15MHz. Increasing the current in this OTA reduces this peak. The noise rise around 1MHz is due to the signal generator.

A selectivity test is performed by simultaneously applying a 5dBm signal at 5MHz and an in-band signal at 1MHz with a 40dB lower level. Figure 3.8.5 shows the measured output spectrum. No spurious tone from the 5MHz signal is observed. The obtained SNDR is 34.3dB. When applying only the desired input signal at 1MHz, the SNDR is 34.4dB. This shows that the ΔΣ ADC can handle high adjacent signals with no degradation of the performances, which is indispensable for digital TV reception. The ΔΣ ADC draws 13.2mA from a 1.8V supply and achieves a 0.7pJ/conversion FOM.

For DVB-T, the ΔΣ ADC is clocked at 100MHz. The achieved peak SNR and SNDR over the 4MHz bandwidth are 73.2dB and 70.1 dB, respectively, but the current consumption is increased to 19.1mA. The FOM is 1.64pJ/conversion.

Figure 3.8.6 summarizes the performances of the ΔΣ ADC and its micrograph is shown in Fig. 3.8.7.

References:

[1] J. Silva, et al., "Wideband Low-Distortion ΔΣ ADC Topology," *Electronics Letters*, pp. 737-738, June, 2001.

[2] A.A. Hamoui, and K.W. Martin, "High-Order Multibit Modulators and Pseudo Data-Weighted-Averaging in Low-Oversampling ΔΣ ADCs for Broad-Band Applications," *IEEE Trans. Circuits Syst. I*, pp. 72-85, Jan., 2004.

[3] E. Siragusa and I. Galton, "A Digitally Enhanced 1.8-V 15-bit 40-Msample/s CMOS Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no.12, pp. 2126-2138, Dec., 2004.

[4] L. Yao, et al., "1-V 140-μW 88-dB Audio Sigma-Delta Modulator in 90-nm CMOS" *IEEE J. Solid-State Circuits*, vol. 39, no.11, pp. 1809-1818, Nov., 2004.

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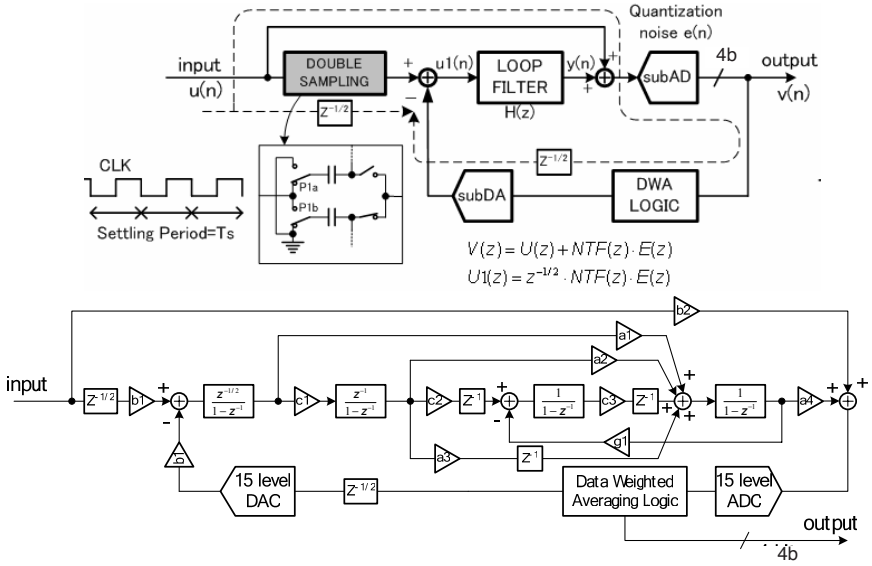

Figure 3.8.1: Architecture and block diagram of the ΔΣ ADC.

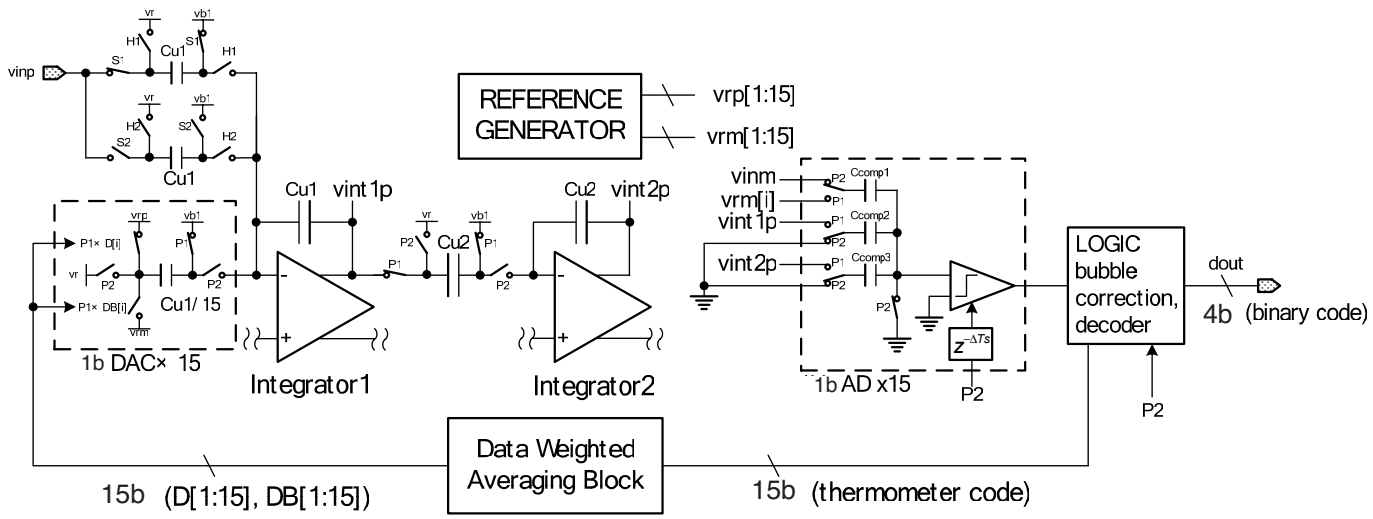

Figure 3.8.2: SC implementation of the ΔΣ modulator.

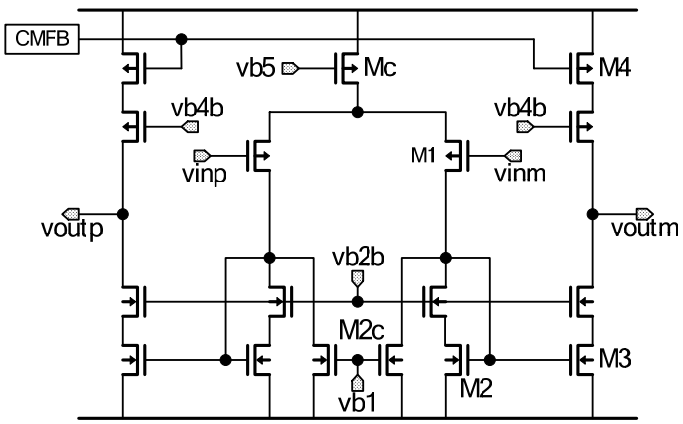

Figure 3.8.3: Current-mirror OTA used in the 1st and 4th integrators.

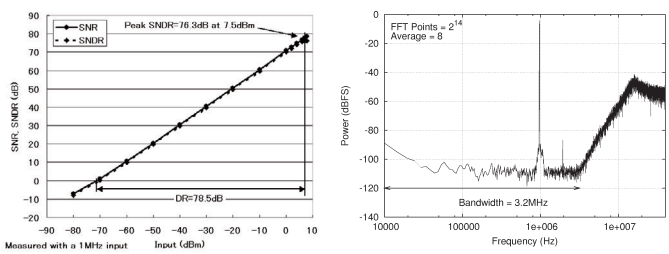

Figure 3.8.4: Measured SNDR curve and spectrum for the maximum input.

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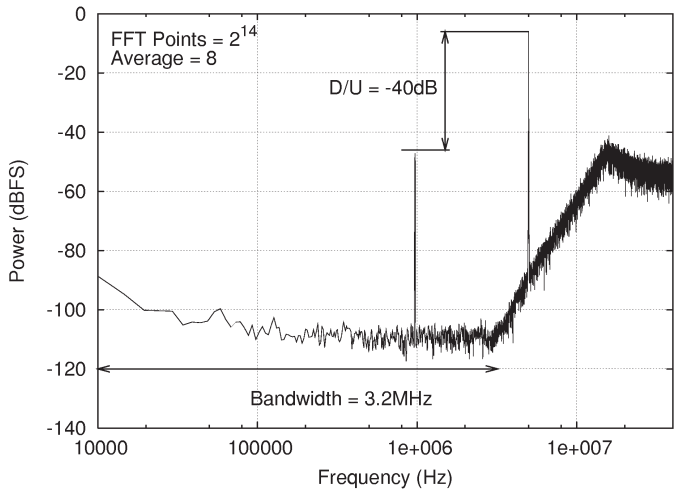

Figure 3.8.5: Selectivity test with a -40dB D/U.

	ISDB-T	DVB-T
Signal Bandwidth	3.2MHz	4MHz
Sampling Frequency	80MHz	100MHz
Dynamic Range	78.5dB	73dB
Peak SNR (for a 1MHz input)	78.2dB	73.2dB
Peak SNDR (for a 1MHz input)	76.3dB	70.1dB
I/Q isolation	> 80dB	
Current Consumption (per 1 channel)	13.2mA at 1.8V	19.1mA at 1.8V
Die Area (per 1 channel)	1.7mm^2	
Technology	0.18μm, 1P5M CMOS	
FOM	0.7pJ/conversion	1.64pJ/conversion

$$FOM = \frac{Power}{2 \cdot BW \times 2^{ENOB}}$$

Figure 3.8.6: Summary of measured performance.

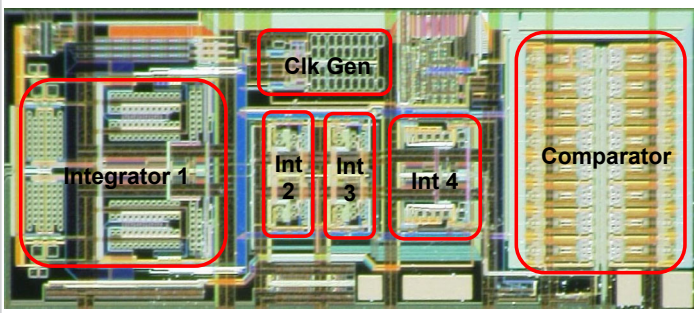

Figure 3.8.7: Chip micrograph.